REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
C	Add generic part number 5537 as device type 02. Add vendor CAGE 18324. Add case ouitline letter P. Make changes to 1.2.1, 1.2.2, 1.3, TABLE I, and FIGURE 1. Redrawn.	94-04-19	M. A. FRYE

DEVICE TYPE 01 IS INACTIVE FOR
NEW DESIGN AS OF 15 DECEMBER 1987.
USE M38510/12501.

REV																				
SHEET																				
REV																				
SHEET																				

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
RICK C. OFFICER

CHECKED BY
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APPROVED BY
MICHAEL A. FRYE

DRAWING APPROVAL DATE
87-06-17

REVISION LEVEL
C

DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, SAMPLE AND HOLD, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-87608**

SHEET 1 OF 13

DESC FORM 193
JUL 91

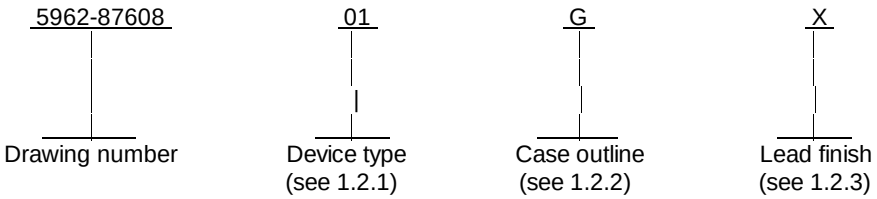
5962-E192-94

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	LF198	Sample and hold
02	5537	Sample and hold

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
G	MACY1-X8	8	Can
P	GDIP1-T8 or CDIP2-T8	8	Dual-in-line

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage ($\pm V_{CC}$) . . . . . ±18 V
Power dissipation (P_D) . . . . . 500 mW
Input voltage (V_{IN}) . . . . . ±18 V 1/
Logic to logic differential voltage . . . . . +7 V, -30 V 2/
Output short circuit duration . . . . . Indefinite
Hold capacitor short circuit duration . . . . . 10 seconds
Lead temperature (soldering, 10 seconds) . . . . . 300°C
Storage temperature range . . . . . -65°C to +150°C
Junction temperature (T_J) . . . . . +150°C
Thermal resistance, junction-to-case (Θ_{JC}) . . . . . See MIL-STD-1835
Thermal resistance, junction-to-ambient (Θ_{JA}):
Case G . . . . . 150°C/W
Case P . . . . . 120°C/W

1.4 Recommended operating conditions.

Supply voltage ($\pm V_{CC}$) . . . . . ±15 V
Ambient operating temperature range (T_A) . . . . . -55°C to+125°C

1/ The maximum input voltage shall not exceed the power supply voltage.
2/ Although the differential voltage may not exceed the limits given, the common-mode voltage the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2 V below the positive supply and 3 V above the negative supply.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram(s). The logic diagram(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Input offset voltage	V_{OS}	$+V_{CC}$ = 3 V, $-V_{CC}$ = -7 V	1	01	-3	3	mV
			2,3		-5	5	
		$\pm V_{CC}$ = 15 V	1		-3	3	
			2,3		-5	5	
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -26.5 V	1		-3	3	
			2,3		-5	5	
		$\pm V_{CC}$ = ±18 V	1		-3	3	
			2,3		-5	5	
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V	1		-3	3	
			2,3		-5	5	
		$+V_{CC}$ = 26.5 V, $-V_{CC}$ = -3.5 V	1		-3	3	
			2,3		-5	5	
		$+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V	1		-3	3	
			2,3		-5	5	
		$+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V	1		-3	3	
			2,3		-5	5	
		$\pm V_{CC}$ = ±5 V to ±18 V	1	02	-3	3	
			2,3		-5	5	
Positive supply current	$+I_{CC}$	V_{CC} = ±15 V	1,2	01		5.5	mA
			3			6.5	
		V_{CC} = ±18 V	1,2	02		6.5	
			3			7.5	
		V_{CC} = ±18 V, mode = sample	1,2	01		5.5	
			3			6.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Positive supply current	$+I_{CC}$	V_{CC} = ±18 V, mode = hold	1,2	01		5.5	mA
			3			6.5	
Negative supply current	$-I_{CC}$	V_{CC} = ±15 V	1,2	01	-5.5		mA
			3		-6.5		
		V_{CC} = ±18 V	1,2	02	-6.5		
			3		-7.5		
		V_{CC} = ±18 V, mode = sample	1,2	01	-5.5		
			3		-6.5		
		V_{CC} = ±18 V, mode = hold	1,2		-5.5		
			3		-6.5		
Input bias current	I_{IB}	$+V_{CC}$ = 3 V, $-V_{CC}$ = -7 V	1	01	-25	25	nA
			2,3		-75	75	
		±V_{CC} = 15 V	1		-25	25	
			2,3		-75	75	
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V	1		-25	25	
			2,3		-75	75	
		$+V_{CC}$ = +32.5 V $-V_{CC}$ = -3.5 V	1		-25	25	
			2,3		-75	75	
		$+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V	1		-25	25	
			2,3		-75	75	
		±V_{CC} = ±5 V to ±18 V	1	02	-25	25	
			2,3		-75	75	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Leakage current into 3/ hold capacitor	I_{LEAK}	$+V_{CC}$ = 3 V, $-V_{CC}$ = -7 V, T_A = +25°C	1	01	-100	100	pA
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V, T_A = +25°C			-100	100	
		$+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V, T_A = +25°C			-100	100	
		$+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V, T_A = +25°C			-100	100	
		Hold mode	1	02		.05	nA
			2,3			25	
Hold step 4/	V_{HS}	$\pm V_{CC}$ = 15 V	1	01	-2	2	mV
			2,3		-5.6	5.6	
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -26.5 V	1		-2.5	2.5	
			2,3		-5.6	5.6	
		$+V_{CC}$ = 26.5 V, $-V_{CC}$ = -3.5 V	1		-2.5	2.5	
			2,3		-5.6	5.6	
		V_{OUT} = 0 V, T_A = +25°C, C_H = 0.01 µF	1	02		2.0	
Input impedance	Z_{IN}	$+V_{CC}$ = 8 V, $-V_{CC}$ = 28 V	1	01	10		GΩ
			2,3		.8		
		$+V_{CC}$ = 28 V, $-V_{CC}$ = -8 V	1		10		
			2,3		.8		
Output impedance	Z_{OUT}	$\pm V_{CC}$ = ±18 V	1	01		2	GΩ
			2,3			4	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Output impedance	Z_{OUT}	Hold mode	1	02		2	Ω
			2,3			4	
Capacitor charging current	I_{CHRG}	$+V_{CC}$ = 8 V, $-V_{CC}$ = -28 V	1	01	-25	-4.5	mA
			2,3		-25	-3	
		$+V_{CC}$ = 28 V, $-V_{CC}$ = -8 V	1		4.5	25	
			2,3		3	25	
Logic pin current	LOGIC	$\pm V_{CC}$ = ±18 V, mode = sample	1,2,3	01	10		µA
		$\pm V_{CC}$ = ±18 V, mode = sample	1			1	
			2,3			.5	
Input offset voltage	V_{OS}	$\pm V_{CC}$ = ±15 V, 1Drive = +1 mA	1	01	-3.5	3.5	mV
	ΔV_{OS}		2,3		-6	6	
		$\pm V_{CC}$ = ±15 V, 1Drive = +1 mA to -1 mA	1		-1.1	1.1	
			2,3		-2	2	
Output short circuit current	$+I_{OS}$	$\pm V_{CC}$ = ±18 V, T_A = +25°C	1	01	7	20	mA
	$-I_{OS}$	$\pm V_{CC}$ = ±18 V, T_A = +25°C			-25	7	
Logic reference pin current	I_{LOG}	$\pm V_{CC}$ = ±18 V, mode = sample	1	01	-1	1	µA
			2,3		-.5	5	
		$\pm V_{CC}$ = ±18 V, mode = hold	1,2,3			10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Logic and logic reference input current	I_{LOG}	V_{IN} = 2.4 V	1	02		10	µA
			2,3			20	
		V_{IN} = 0 V	1		-10		
			2,3		-20		
Power supply rejection ratio	PSRR	$+V_{CC}$ = 10 V, $-V_{CC}$ = -15 V	1	01	80		dB
			2,3		74		
		$+V_{CC}$ = 15 V, $-V_{CC}$ = -10 V	1		80		
			2,3		74		
		$+V_{CC}$ = 15 V, V_{OUT} = 0 V, $-V_{CC}$ = -10 V	1,2,3	02	80		
Feedthrough rejection ratio	FTRR	$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V	1	01	86		dB
			2,3		74		
		$+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V	1		86		
			2,3		74		
Feedthrough attenuation ratio	FTAR	C_H = 0.01 µF, T_A = +25°C	1	02	86		dB
Differential logic level 5/	V_{TH}	T_A = +25°C	1	All	.8	2.4	V
Second stage V_{OS}	V_{OS} (2nd stage)	$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -32.5 V	1	01	-35	35	mV
			2,3		-50	50	
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = -7 V	1		-35	35	
			2,3		-50	50	
		$+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V	1		-35	35	
			2,3		-50	50	
		$+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V	1		-35	35	mV
			2,3		-50	50	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Acquistion time 6/	t_{AQ}	ΔV_{OUT} = 10 V, T_A = +25°C, C_{HOLD} = 1000 pF	4	01		6	µs
		ΔV_{OUT} = 10 V, T_A = +25°C, C_{HOLD} = .01 µF				25	
Gain error	A_E	$+V_{CC}$ = 7 V, $-V_{CC}$ = -3 V	4	01		.02	%
			5,6			.06	
		$+V_{CC}$ = 3.5 V, $-V_{CC}$ = 26.5 V	4			.005	
			5,6			.02	
		$+V_{CC}$ = 32.5 V, $-V_{CC}$ = -3.5 V	4			.005	
			5,6			.06	
		$+V_{CC}$ = 26.5 V, $-V_{CC}$ = 3.5 V	4			.005	
			5,6			.02	
		V_{IN} = -10 V to 10 V, R_L = 2 kΩ	4	02		.007	
			5,6			.01	
		V_{IN} = -11.5 to 11.5 V, R_L = 10 kΩ	4			.007	
			5,6			.01	

1/ Unless otherwise specified, V_{CC} = ±15 V, C_{HOLD} = 0.01 µF, and logic reference pin = 0 V. For device type 01, R_L = 10 kΩ and V_{IN} = 0 V. For device type 02, R_L = 2 kΩ, V_{IN} = -11.5 V to +11.5 V and logic voltage = 2.5 V.

2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal

3/ Leakage current is measured at a junction temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

4/ Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. One pF, for instance, will create an additional 0.5 mV step with 5 V logic swing and a 0.01 µF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

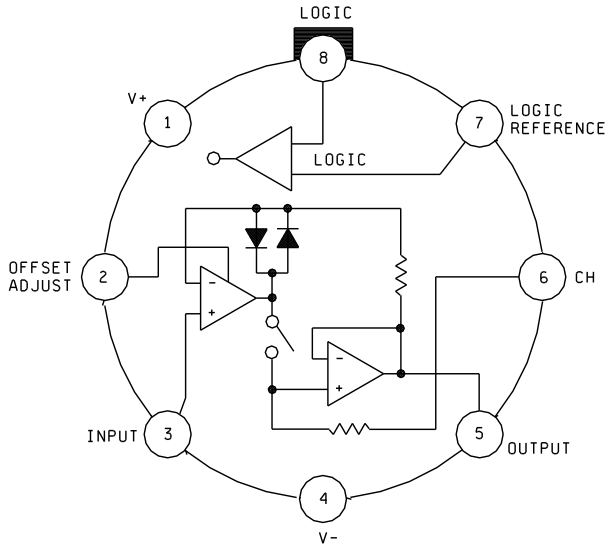
5/ Parameter tested go-no-go only.

6/ If not tested, shall be guaranteed to the limits specified in table I herein.

Device types	01	02
Case outlines	G	P
Terminal number	Terminal symbol	
1	$+V_{CC}$	$+V_{CC}$
2	OFFSET ADJUST	OFFSET ADJUST
3	+INPUT	+INPUT
4	$-V_{CC}$	$-V_{CC}$
5	OUTPUT	OUTPUT
6	C_H	C_H
7	LOGIC REFERENCE	LOGIC REFERENCE
8	LOGIC	LOGIC

FIGURE 1. Terminal connections.

Device type 01



Device type 02

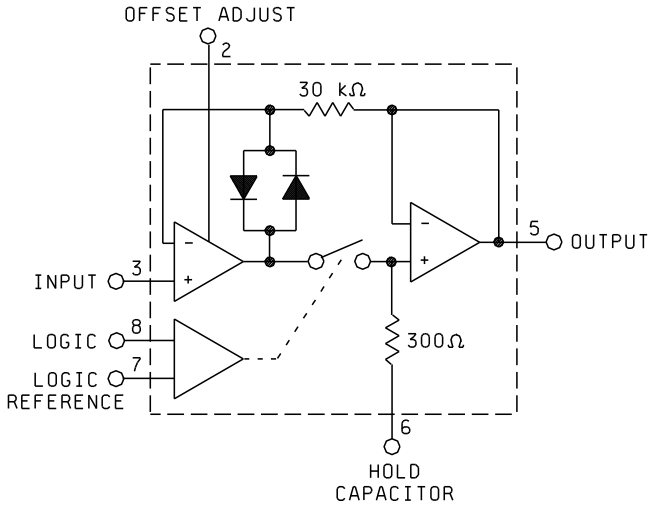


FIGURE 2. Logic diagrams.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*,2,3,4
Group A test requirements (method 5005)	1,2,3,4,5,6
Groups C and D end-point electrical parameters (method 5005)	1,2,3,4,5,6

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part nuimbered device specified in this drawing will be replaced by the microcircuit identified as part numbers M38510/12501 and M38510/12502.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 94-04-19

Approved sources of supply for SMD 5962-87608 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-EC. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Standardized military drawing PIN	Vendor CAGE number	Vendor similar PIN 1/	Replacement military specification part number
5962-8760801GX	27014	LF198H/883B	M38510/12501BGX
5962-8760802PX	18324	5537/BPA	M38510/12502BPX

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
18324	Philips 811 E. Arques Avenue P.O. Box 3409 Sunnyvale, CA 94088-3409
27014	National Semiconductor Corporation 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95051-8090